

1 What is claimed is:

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3 1. A timing recovery loop for generating adjusted timing pulses  
4 from a baseband signal waveform encoding a self clocking  
5 digital bit stream, the timing recovery loop comprising,  
6       a pulse detector for generating data transition pulses from  
7 the baseband signal waveform, for comparing the data transition  
8 pulses with the adjusted timing pulses for generating early  
9 signals and lag signals

10       a random walk counter for counting the early signals and lag  
11 signals for generating a running count,

12       a threshold comparator for determining when the running  
13 count exceeds a predetermined threshold value, and

14       a timing pulse delay adjustor for delaying the adjusted  
15 timing pulses for synchronizing the adjusted timing pulses with  
16 the data transition pulses when the running count exceeds the  
17 predetermined threshold value.

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19 2. The timing recovery loop of claim 1 further comprising,

20       a data detector for generating a reconstructed digital bit  
21 stream by sampling the baseband signal waveform by the adjusted  
22 timing pulses.

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26 3. The timing recovery loop of claim 1 further comprising,  
27       a threshold value selector for selecting the threshold  
28 value.

1       4. The timing recovery loop of claim 1 further comprising,  
2            a threshold value selector for selecting the threshold  
3            value, and  
4            an adaptive means for monitoring the rate at which the  
5            timing pulse delay is adjusted, the threshold value selector  
6            adaptively selecting different threshold values when the  
7            adjustment rate exceeds a predetermined rate.

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14       5. The timing recovery loop of claim 1 further comprising,  
15            a count magnitude generator for generating the magnitude  
16            count from the running count, the magnitude count being fed to  
17            the threshold comparator for determining when the running count  
18            exceeds the predetermined threshold value, and  
19            a count sign clipper for generating a count sign from the  
20            running count, the count sign being fed to the timing pulse  
21            delay adjustor for generating a timing pulse delay to adjust  
22            the adjusted timing pulses, the sign count for increasing the  
23            timing pulse delay when the data transition pulses arrive late  
24            relative to the adjusted timing pulses and for decreasing the  
25            timing pulse delay when the data transition pulses arrive early  
26            relative to the adjusted timing pulses.

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1       6. The timing recovery loop of claim 1 wherein the pulse  
2       detector comprises,

3              a data transition pulse generator for generating the data  
4       transition pulses,

5              a timing delay for delaying reference timing pulses into  
6       the adjusted timing pulses, and

7              a lead and lag generator for generating lead and lag  
8       signals for early and late arrivals of the data transition  
9       pulses relative to the adjusted timing pulses.

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13       7. The timing recovery loop of claim 1 wherein the pulse  
14       detector comprises,

15              a data transition pulse generator for generating the data  
16       transition pulses,

17              a timing delay for delaying reference timing pulses into  
18       the adjusted timing pulses, and

19              a data transition pulse counter for counting the number of  
20       data transition pulses within a search window following an  
21       adjusted timing pulse, and

22              a lead and lag generator for generating lead and lag  
23       signals for early and late arrivals of the data transition  
24       pulses relative to the adjusted timing pulses when one and only  
25       one data transition pulse occurs within each search window  
26       following an adjusted timing pulse.

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1       8. The timing recovery loop of claim 1 wherein the pulse  
2       detector comprises,

3             a data transition pulse generator for generating the data  
4       transition pulses,

5             a window delay for delaying the data transition pulses by  
6       half of a search window to center the data transition pulses  
7       within respective search windows,

8             a timing delay for delaying by a timing pulse delay the  
9       reference timing pulses into the adjusted timing pulses, the  
10      timing pulse delay being generated by the timing delay  
11      adjustor, the timing pulse delay being adjusted when the  
12      running count exceeds predetermined threshold value,

13             a data transition pulse counter for counting the number of  
14       data transition pulses within the search window following an  
15       adjusted timing pulse, and

16             a lead and lag generator for generating lead and lag  
17       signals for early and late arrivals of the data transition  
18       pulses relative to the adjusted timing pulses when one and only  
19       one data transition pulse occurs within a respective one of the  
20       search windows following a respective one of the adjusted  
21       timing pulses.

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